JMF602
SATA II to Flash controller
Datasheet

Ver. 1.7

Revision History

Version	Date	Revision Description
1.0	2008/08/01	Final Release
1.1	2008/08/22	Modify page.12:GPIO4 pin definition.
1.2	2008/09/12	add page.17:ECC descriptions.
1.3	2008/10/17	Add page35 10.2 ambient operation temperature for industry.
1.4	2008/11/14	Add 10.2 Recommended Power Supply Operation Conditions and Temperature
1.5	2008/12/03	Add 2.6 Firmware Modify page13 60MHz internal Clock select (H-60MHz, L-75MHz). Modify page 5 (2.FLASH) Maximum CEs support . Modify page6 (4.Total capacity) table.
1.6	2009/02/02	ATA command register modified.
1.7	2009/03/04	ATA command register modified.

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1. General Description

JMF602 is a single chip, supports SATA II and USB2.0 to NAND flash interface. It is native design to provide higher bandwidth for flash memory access.

JMF602 can support the maximum read and write speed to drive the limit of flash memory. JMF602 has the best supporting to the latest NAND flash memory, including Samsung, Toshiba, Hynix, Micron and IM Flash. It also provides the embedded hardware error correction code (ECC), wear leveling, and bad block management technology in this chip. In order to resolve compatibility issue, JMF602 provides the on line firmware upgrade ability.

JMF602 provides embedded processor, internal masked ROM, data SRAM, SATA link/transport layer, SATA PHY, USB 2.0 device controller and USB 2.0 PHY. Data swap between different interfaces can be done very efficiency by DMA without CPU involvement. Based on the efficient architecture, the JMF602 can provide the best performance.

2. Features

2.1 Compliance

- Compliant with Universal Serial Bus Specification Revision 2.0.
- Compliant with USB Mass Storage Class specification version 1.0.
- Compliant with Serial ATA International Organization: Serial ATA Revision 2.6.

2.2 SATA I/II

- Supports 1-port 1.5/3.0Gbps SATA I/II interface

2.3 CPU

- Embedded processor
- Embedded masked program ROM
- Embedded system RAM

2.4 FLASH

- Support maximum CEs to 64 CEs
- Enhanced endurance by dynamic/static wear-leveling
- Supports 2K/4K bytes page size
- Supports dynamic power management
- SMART (Self-Monitoring, Analysis and Reporting Technology)
- Data integrity under power-cycling
- Supports online USB firmware update
- Supports 8 bits Flash interface
- Supports BCH ECC 8 bits or 15bits in 512 bytes

2.5 SYSTEM

- Integrated 1-USB2.0 port, 1-SATA II port and 4-channels Flash controller.
- LED indicator for USB2.0 and SATA read/write access.
- LED indicator for USB2.0 and SATA PHY link up.
- Provides 6 GPIO pins for customer.
- Provides UART and JTAG for S/W debugging.
- Built-in power-up self-test (BIST).
- Manual and automatic self-diagnostics.
- Provides voltage low detect interrupt.
- 211-ball TFBGA package

2.6 Firmware

- Support NCQ on this controller.
- Support LBA24 & LBA48 on this controller.
- Support 1 to 8 banks selected free.

- Support 2 to 8 channels selected free.

3. Block Diagram

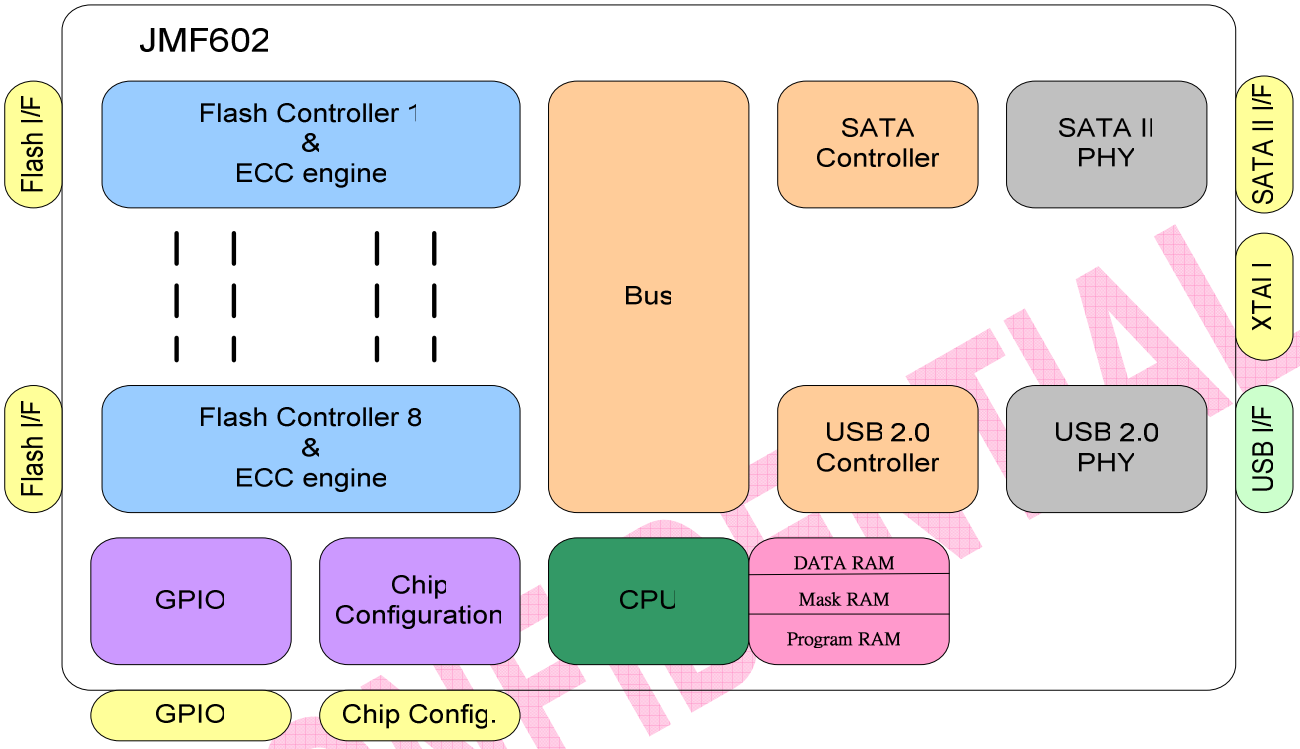


Figure 1: JMF602 Block Diagram

4. Total capacity

density/per flash	Support CE pins/per flash	maximum flash number	Total capacity
1G x 8 Bits (8Gb)	1 CE pin	32	32G Bytes
2G x 8 Bits (16Gb)	1 CE/ 2 CE pin	32	64G Bytes
4G x 8 Bits (32Gb)	1 CE/ 2 CE pin	32	128G Bytes
8G x 8 Bits (64Gb)	2 CE pin	32	256G Bytes
16G x 8 Bits (128Gb)	4 CE pin	16	256G Bytes

Table 1: JMF602 Total capacity table

5. Package Pin out

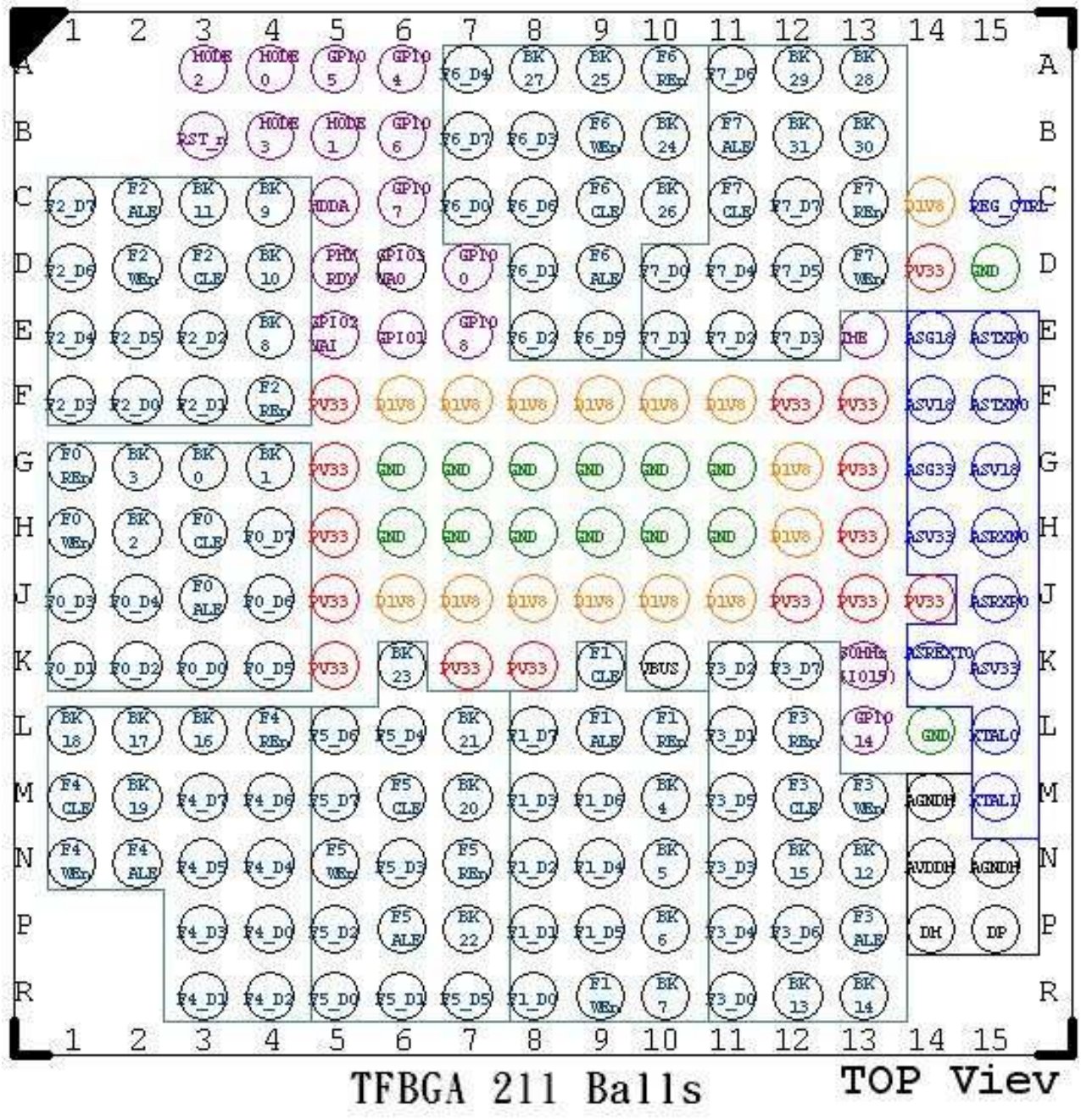


Figure 2: Package Ball Assignment of JMF602

6. Package outline (JMF602)

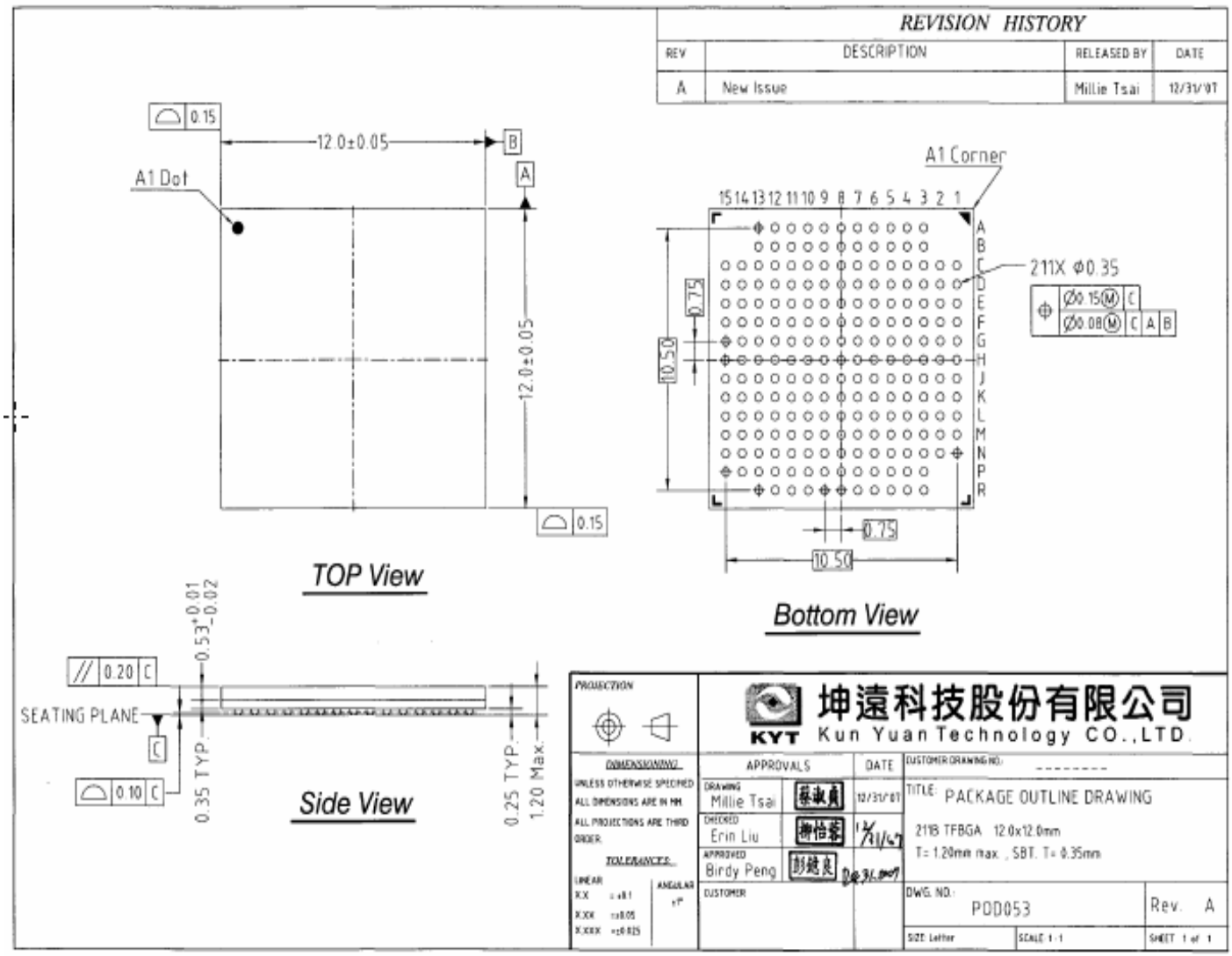


Figure 3: Package outline of JMF602.

7. Pin Descriptions

7.1 Pin Type Definition

Pin Type	Definition
A	Analog
D	Digital
I	Input
O	Output
IO	Bi-directional
IL	Internal week pull-low (Typical 75KΩ)
IH	Internal week pull-high (Typical 75KΩ)

7.2 Pin definition

Signal Name	Ball No.	Type	Description
F5_D0	R5	IO	**Flash data input0/output0** The I/O pins are used to output command, address, data and to input data during read operations.
F5_D1	R6	IO	**Flash data input1/output1** The I/O pins are used to output command, address, data and to input data during read operations.
F5_D2	P5	IO	**Flash data input2/output2** The I/O pins are used to output command, address, data and to input data during read operations.
F5_D3	N6	IO	**Flash data input3/output3** The I/O pins are used to output command, address, data and to input data during read operations.
F5_D4	L6	IO	**Flash data input4/output4** The I/O pins are used to output command, address, data and to input data during read operations.
F5_D5	R7	IO	**Flash data input5/output5** The I/O pins are used to output command, address, data and to input data during read operations.
F5_D6	L5	IO	**Flash data input6/output6** The I/O pins are used to output command, address, data and to input data during read operations.
F5_D7	M5	IO	**Flash data input7/output7** The I/O pins are used to output command, address, data and to input data during read operations.
F5WEn	N5	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WEn pulse
F5ALE	P6	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.

Signal Name	Ball No.	Type	Description
F5CLE	M6	O	**Command Latch Enable** The CLE output controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
BK23n	K6	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK22n	P7	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK21n	L7	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK20n	M7	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
F5REn	N7	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.
F1_D0	R8	IO	**Flash data input0/output0** The I/O pins are used to output command, address, data and to input data during read operations.
F1_D1	P8	IO	**Flash data input1/output1** The I/O pins are used to output command, address, data and to input data during read operations.
F1_D2	N8	IO	**Flash data input2/output2** The I/O pins are used to input command, address, data and to output data during read operations.
F1_D3	M8	IO	**Flash data input3/output3** The I/O pins are used to output command, address, data and to input data during read operations.
F1_D4	N9	IO	**Flash data input4/output4** The I/O pins are used to output command, address, data and to input data during read operations.
F1_D5	P9	IO	**Flash data input5/output5** The I/O pins are used to output command, address, data and to input data during read operations.
F1_D6	M9	IO	**Flash data input6/output6** The I/O pins are used to output command, address, data and to input data during read operations.
F1_D7	L8	IO	**Flash data input7/output7** The I/O pins are used to output command, address, data and to input data during read operations.

Signal Name	Ball No.	Type	Description
F1WEn	R9	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse
F1ALE	L9	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
F1CLE	K9	O	**Command Latch Enable** The CLE output controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
BK7n	R10	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK6n	P10	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK5n	N10	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK4n	M10	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
F1REn	L10	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.
VBUS	K10	DIL	**USB Cable Power Detector.** The 51KΩ and 100KΩ resistances should be connected to divide the 5V cable power into 3.3V.
F3_D0	R11	IO	**Flash data input0/output0** The I/O pins are used to output command, address, data and to input data during read operations.
F3_D1	L11	IO	**Flash data input1/output1** The I/O pins are used to output command, address, data and to input data during read operations.
F3_D2	K11	IO	**Flash data input2/output2** The I/O pins are used to output command, address, data and to input data during read operations.
F3_D3	N11	IO	**Flash data input3/output3** The I/O pins are used to output command, address, data and to input data during read operations.

Signal Name	Ball No.	Type	Description
F3_D4	P11	IO	**Flash data input4/output4** The I/O pins are used to output command, address, data and to input data during read operations.
F3_D5	M11	IO	**Flash data input5/output5** The I/O pins are used to output command, address, data and to input data during read operations.
F3_D6	P12	IO	**Flash data input6/output6** The I/O pins are used to output command, address, data and to input data during read operations.
F3_D7	K12	IO	**Flash data input7/output7** The I/O pins are used to output command, address, data and to input data during read operations.
F3WEn	M13	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WEn pulse
F3ALE	P13	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
F3CLE	M12	O	**Command Latch Enable** The CLE output controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
BK15n	N12	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK14n	R13	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK13n	R12	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK12n	N13	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
F3REn	L12	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.
GPIO14	L13	DIO	**General purpose I/O,** Can be configured by customer firmware.
60MHz	K13	DI	**Internal clock,** Def. Pull-L. (H-60MHz, L-75MHz)

Signal Name	Ball No.	Type	Description
DM	P14	AIO	**USB Bus D- Signal.**
DP	P15	AIO	**USB Bus D+ Signal.**
AVDDH	N14	AI	**USB Analog 3.3V Power Supply.**
AGNDH	N15/M14	AI	**USB Analog Ground**
XTALI	M15	AI	**Crystal input pad** It is connected to a 30MHz crystal.
XTALO	L15	AO	**Crystal output pad** It is connected to a crystal.
ASV33	H14/K15	AI	**SATA Analog 3.3V Power Supply.**
ASG33	G14	AI	**SATA Analog Ground.**
ASREXT0	K14	AI	**External Reference Resistance.** A 12KΩ±1% external resistor should be connected to this pin.
ASRXP0	J15	AI	**Serial ATA RX+ signal.** A 10nF CAP. should be connected between this pin and SATA connector.
ASRXN0	H15	AI	**Serial ATA RX- signal.** A 10nF CAP. should be connected between this pin and SATA connector.
ASV18	G15/F14	AI	**SATA Analog 1.8V Power Supply.** This power could be sourced from internal 1.8V voltage regulator through AVREG pin.
ASG18	E14	AI	**SATA Analog Ground.**
ASTXN0	F15	AO	**Serial ATA TX- signal.** A 10nF CAP. should be connected between this pin and SATA connector.
ASTXP0	E15	AO	**Serial ATA TX+ signal.** A 10nF CAP. should be connected between this pin and SATA connector.
REG_CTRL	C15	AO	**Voltage Regulator control.**
TMEn	E13	DIH	**Test Mode Enable, (internal pull-H)** This pin is reserved for IC mass production testing. Always Keep this pin to logic “1” in normal operation.
F7_D0	D10	IO	**Flash data input0/output0** The I/O pins are used to output command, address, data and to input data during read operations. Write Enable
F7_D1	E10	IO	**Flash data input1/output1** The I/O pins are used to output command, address, data and to input data during read operations. Write Enable
F7_D2	E11	IO	**Flash data input2/output2** The I/O pins are used to output command, address, data and to input data during read operations. Write Enable.
F7_D3	E12	IO	**Flash data input3/output3** The I/O pins are used to output command, address, data and to input data during read operations. Write Enable.

Signal Name	Ball No.	Type	Description
F7_D4	D11	IO	**Flash data input4/output4** The I/O pins are used to output command, address, data and to input data during read operations. Write Enable.
F7_D5	D12	IO	**Flash data input5/output5** The I/O pins are used to output command, address, data and to input data during read operations. Write Enable.
F7_D6	A11	IO	**Flash data input6/output6** The I/O pins are used to output command, address, data and to input data during read operations. Write Enable.
F7_D7	C12	IO	**Flash data input7/output7** The I/O pins are used to output command, address, data and to input data during read operations. Write Enable.
F7WEn	D13	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WEn pulse
F7ALE	B11	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
F7CLE	C11	O	**Command Latch Enable** The CLE output controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
F7REn	C13	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.
BK31n	B12	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK30n	B13	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK29n	A12	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK28n	A13	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.

Signal Name	Ball No.	Type	Description
F6REn	A10	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.
BK24n	B10	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK25n	A9	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK26n	C10	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK27n	A8	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
F6CLE	C9	O	**Command Latch Enable** The CLE input controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
F6ALE	D9	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
F6WEn	B9	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WEn pulse
F6_D7	B7	IO	**Flash data input7/output7** The I/O pins are used to output command, address, data and to input data during read operations.
F6_D6	C8	IO	**Flash data input6/output6** The I/O pins are used to output command, address, data and to input data during read operations.
F6_D5	E9	IO	**Flash data input5/output5** The I/O pins are used to output command, address, data and to input data during read operations.
F6_D4	A7	IO	**Flash data input4/output4** The I/O pins are used to output command, address, data and to input data during read operations.
F6_D3	B8	IO	**Flash data input3/output3** The I/O pins are used to output command, address, data and to input data during read operations.

Signal Name	Ball No.	Type	Description
F6_D2	E8	IO	**Flash data input2/output2** The I/O pins are used to output command, address, data and to input data during read operations.
F6_D1	D8	IO	**Flash data input1/output1** The I/O pins are used to output command, address, data and to input data during read operations.
F6_D0	C7	IO	**Flash data input0/output0** The I/O pins are used to output command, address, data and to input data during read operations.
GPIO8	E7	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO0	D7	DIO	**General purpose I/O,** For normal function can be configured by customer.
GPIO1	E6	DIO	**General purpose I/O,** For normal function can be configured by customer.
GPIO2/UAI	E5	DIO	**General purpose I/O,** For normal function can be configured by customer.
GPIO3/UAO	D6	DIO	**General purpose I/O,** For normal function can be configured by customer.
GPIO4/Load USB	A6	DIO	**General purpose I/O,(F/W setting)** 0: Run SATA 1.5Gbps. 1: Run SATA 3.0Gbps.
GPIO5/Load Flash	A5	DIO	**General purpose I/O,** 0: Load firmware code from flash to program memory. 1: Load firmware code from host to program memory.
GPIO6	B6	DIO	**General purpose I/O,** Can be configured by customer firmware.
GPIO7	C6	DIO	**General purpose I/O,** Can be configured by customer firmware.
MODE[3:0]	B4/A3/B5/ A4	IL	**Chip Operation Mode Selection.(internal 0000)** Ball B4 A3 B5 A4 0 0 0 0
RSTn	B3	DIH	**System Global Reset Input.** Active-low to reset the entire chip. An external 10msec RC should be connected to this pin.
HDDA	C5	DO	**SATA Hard Disk Active.(GPIO21)** Can be configured by customer firmware.
PHYRDY	D5	DO	**PHYRDY of SATA/USB output.**
F2REn	F4	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.

Signal Name	Ball No.	Type	Description
BK8n	E4	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK9n	C4	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK10n	D4	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK11n	C3	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
F2CLE	D3	O	**Command Latch Enable** The CLE output controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
F2ALE	C2	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
F2WEn	D2	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WEn pulse
F2_D7	C1	IO	**Flash data input7/output7** The I/O pins are used to output command, address, data and to input data during read operations.
F2_D6	D1	IO	**Flash data input6/output6** The I/O pins are used to output command, address, data and to input data during read operations.
F2_D5	E2	IO	**Flash data input5/output5** The I/O pins are used to output command, address, data and to input data during read operations.
F2_D4	E1	IO	**Flash data input4/output4** The I/O pins are used to output command, address, data and to input data during read operations.
F2_D3	F1	IO	**Flash data input3/output3** The I/O pins are used to output command, address, data and to input data during read operations.
F2_D2	E3	IO	**Flash data input2/output2** The I/O pins are used to output command, address, data and to input data during read operations.
F2_D1	F3	IO	**Flash data input1/output1** The I/O pins are used to output command, address, data and to input data during read operations.

Signal Name	Ball No.	Type	Description
F2_D0	F2	IO	**Flash data input0/output0** The I/O pins are used to output command, address, data and to input data during read operations.
F0REn	G1	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.
BK0n	G3	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK1n	G4	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK2n	H2	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK3n	G2	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
F0CLE	H3	O	**Command Latch Enable** The CLE output controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
F0ALE	J3	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
F0WEn	H1	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WEn pulse
F0_D7	H4	IO	**Flash data input7/output7** The I/O pins are used to output command, address, data and to input data during read operations.
F0_D6	J4	IO	**Flash data input6/output6** The I/O pins are used to output command, address, data and to input data during read operations.
F0_D5	K4	IO	**Flash data input5/output5** The I/O pins are used to output command, address, data and to input data during read operations.
F0_D4	J2	IO	**Flash data input4/output4** The I/O pins are used to output command, address, data and to input data during read operations.

Signal Name	Ball No.	Type	Description
F0_D3	J1	IO	**Flash data input3/output3** The I/O pins are used to output command, address, data and to input data during read operations.
F0_D2	K2	IO	**Flash data input2/output2** The I/O pins are used to output command, address, data and to input data during read operations.
F0_D1	K1	IO	**Flash data input1/output1** The I/O pins are used to output command, address, data and to input data during read operations.
F0_D0	K3	IO	**Flash data input0/output0** The I/O pins are used to output command, address, data and to input data during read operations.
F4REn	L4	O	**Read Enable** The REn output is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of REn which also increments the internal column address counter by one.
BK16n	L3	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK17n	L2	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK18n	L1	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
BK19n	M2	O	**Bank Selector** The BKn output is the device selection control. When the device is in the Busy state, BKn high is ignored, and the device does not return to standby mode in program or erase operation.
F4CLE	M1	O	**Command Latch Enable** The CLE output controls the activating path for commands sent to the command registers. When active high, commands are latched into the command register through the I/O ports on the edge of the WEn signal.
F4ALE	N2	O	**Address Latch Enable** The ALE output controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WEn with ALE high.
F4WEn	N1	O	**Write Enable** The WEn output controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WEn pulse
F4_D7	M3	IO	**Flash data input7/output7** The I/O pins are used to output command, address, data and to input data during read operations.

Signal Name	Ball No.	Type	Description
F4_D6	M4	IO	**Flash data input6/output6** The I/O pins are used to output command, address, data and to input data during read operations.
F4_D5	N3	IO	**Flash data input5/output5** The I/O pins are used to output command, address, data and to input data during read operations.
F4_D4	N4	IO	**Flash data input4/output4** The I/O pins are used to output command, address, data and to input data during read operations.
F4_D3	P3	IO	**Flash data input3/output3** The I/O pins are used to output command, address, data and to input data during read operations.
F4_D2	R4	IO	**Flash data input2/output2** The I/O pins are used to output command, address, data and to input data during read operations.
F4_D1	R3	IO	**Flash data input1/output1** The I/O pins are used to output command, address, data and to input data during read operations.
F4_D0	P4	IO	**Flash data input0/output0** The I/O pins are used to output command, address, data and to input data during read operations.
PV33	F5	DI	**I/O Pad 3.3V Power Supply.**
PV33	G5	DI	**I/O Pad 3.3V Power Supply.**
PV33	H5	DI	**I/O Pad 3.3V Power Supply.**
PV33	J5	DI	**I/O Pad 3.3V Power Supply.**
PV33	K5	DI	**I/O Pad 3.3V Power Supply.**
PV33	F12	DI	**I/O Pad 3.3V Power Supply.**
PV33	F13	DI	**I/O Pad 3.3V Power Supply.**
PV33	G13	DI	**I/O Pad 3.3V Power Supply.**
PV33	H13	DI	**I/O Pad 3.3V Power Supply.**
PV33	J12	DI	**I/O Pad 3.3V Power Supply.**
PV33	J13	DI	**I/O Pad 3.3V Power Supply.**
PV33	J14	DI	**I/O Pad 3.3V Power Supply.**
PV33	K7	DI	**I/O Pad 3.3V Power Supply.**
PV33	K8	DI	**I/O Pad 3.3V Power Supply.**
PV33	D14	DI	**I/O Pad 3.3V Power Supply.**
GND	L14	DI	**Ground.**
GND	G6	DI	**Ground.**
GND	G7	DI	**Ground.**
GND	G8	DI	**Ground.**
GND	G9	DI	**Ground.**
GND	G10	DI	**Ground.**
GND	G11	DI	**Ground.**
GND	H6	DI	**Ground.**
GND	H7	DI	**Ground.**
GND	H8	DI	**Ground.**
GND	H9	DI	**Ground.**
GND	H10	DI	**Ground.**
GND	H11	DI	**Ground.**

Signal Name	Ball No.	Type	Description
GND	D15	DI	**Ground.**
DV18	F6	DI	**1.9V Power Supply.**
DV18	F7	DI	**1.9V Power Supply.**
DV18	F8	DI	**1.9V Power Supply.**
DV18	F9	DI	**1.9V Power Supply.**
DV18	F10	DI	**1.9V Power Supply.**
DV18	F11	DI	**1.9V Power Supply.**
DV18	G12	DI	**1.9V Power Supply.**
DV18	H12	DI	**1.9V Power Supply.**
DV18	J6	DI	**1.9V Power Supply.**
DV18	J7	DI	**1.9V Power Supply.**
DV18	J8	DI	**1.9V Power Supply.**
DV18	J9	DI	**1.9V Power Supply.**
DV18	J10	DI	**1.9V Power Supply.**
DV18	J11	DI	**1.9V Power Supply.**
DV18	C14	DI	**1.9V Power Supply.**

8. ECC Descriptions

Please refer to FIG. 4 that is a diagram illustrating an allocating method of a spare area in each page of a NAND flash memory, where in the specific ECC algorithm utilizes a Bose, Chaudhuri and Hocquengham (BCH) ECC algorithm. When a BCH 8 ECC algorithm encodes the data in the NAND flash memory, the parity code generated in the encoding process may occupy 13 bytes of the spare area in each page. When a BCH 15 ECC algorithm encodes the data in the NAND flash memory, the parity code generated in the encoding process may occupy 25 bytes of the spare area in each page.

When a BCH 8 algorithm decodes the data in the NAND flash memory, the data can be decoded correctly if the error bit happened in one sector (512Bytes) is 8. When a BCH 15 algorithm decodes the data in the NAND flash memory, the data can be decoded correctly if the error bit happened in one sector is 15.

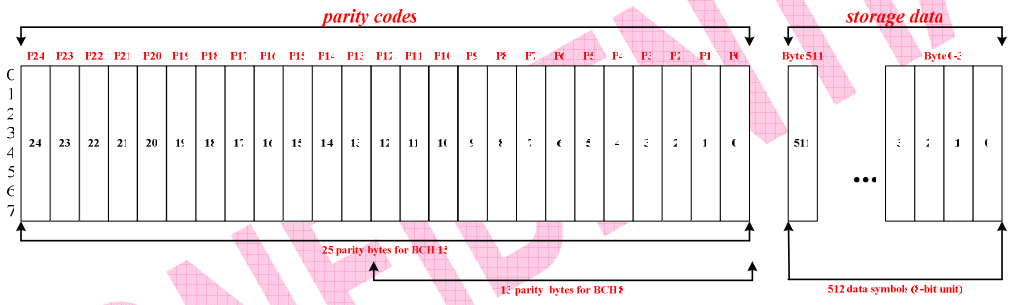


Figure 4. Allocation for ECC Algorithm BCH in NAND Flash

9. SATA Interface

9.1 Out of bank signaling

There shall be three Out Of Band (OOB) signals used/detected by the Phy: COMRESET, COMINIT, and COMWAKE. COMINIT, COMRESET and COMWAKE OOB signaling shall be achieved by transmission of either a burst of four Gen1 $ALIGN_P$ primitives or a burst composed of four Gen1 Dwords with each Dword composed of four D24.3 characters, each burst having duration of 160 UI_{OOB}. Each burst is followed by idle periods (at common-mode levels), having durations as depicted in Figure 5 and Table 2.

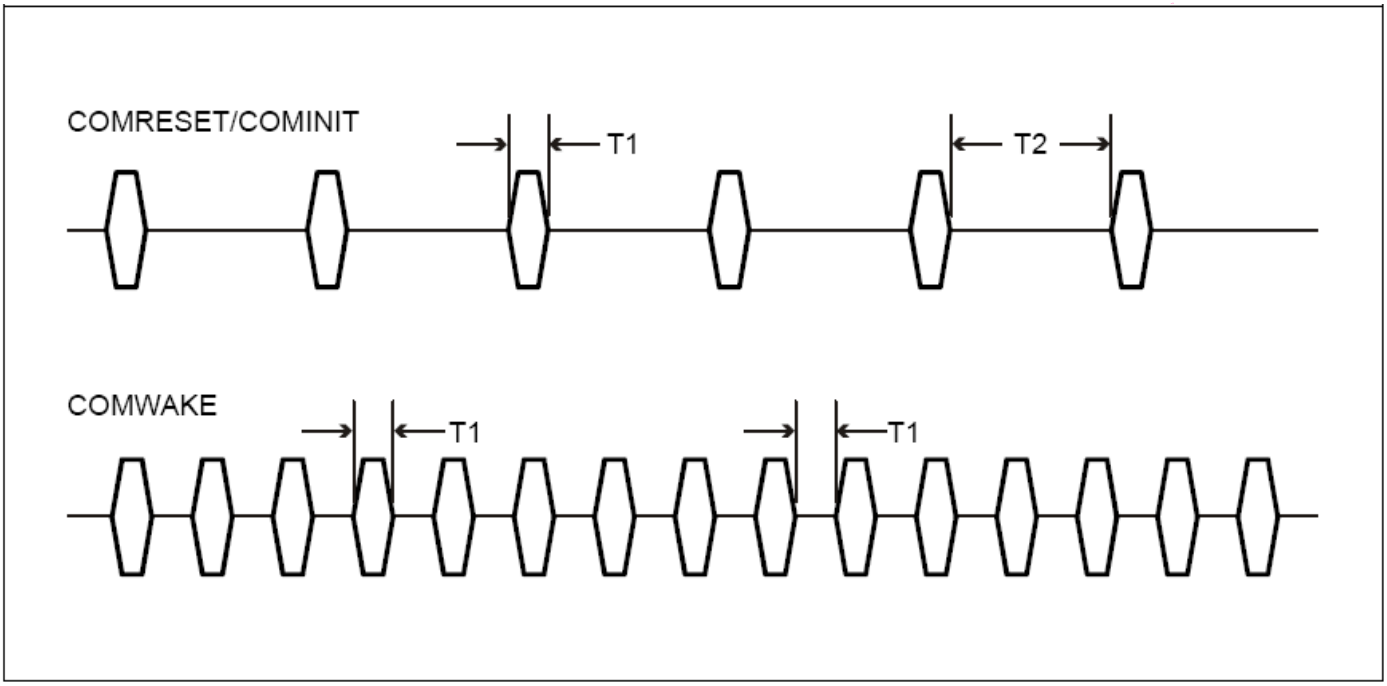


Figure 5 : OOB signals

Time	Value
T1	160 UI_{oob} (106.7 ns nominal)
T2	480 UI_{oob} (320 ns nominal)

Table 2 : OOB signal times

9.2 COMRESET

COMRESET always originates from the host controller, and forces a hardware reset in the device. It is indicated by transmitting bursts of data separated by an idle bus condition. The OOB COMRESET signal shall consist of no less than six data bursts, including inter-burst temporal spacing.

The COMRESET signal shall be:

1) Sustained/continued uninterrupted as long as the system hard reset is asserted, or 2) Started during the system hardware reset and ended some time after the negation of system hardware reset, or 3) Transmitted immediately following the negation of the system hardware reset signal.

The host controller shall ignore any signal received from the device from the assertion of the hardware reset signal until the COMRESET signal is transmitted. Each burst shall be 160 Gen1 UI's long (106.7 ns) and each inter-burst idle state shall be 480 Gen1 UI's long (320 ns). A COMRESET detector looksfor four consecutive bursts with 320 ns spacing (nominal). Any spacing less than 175 ns or greater than 525 ns shall invalidate the COMRESET detector output. The COMRESET interface signal to the Phy layer shall initiate the Reset sequence shown in Figure 6 below. The interface shall be held inactive for at least 525 ns after the last burst to ensure far-end detector detects the negation properly.

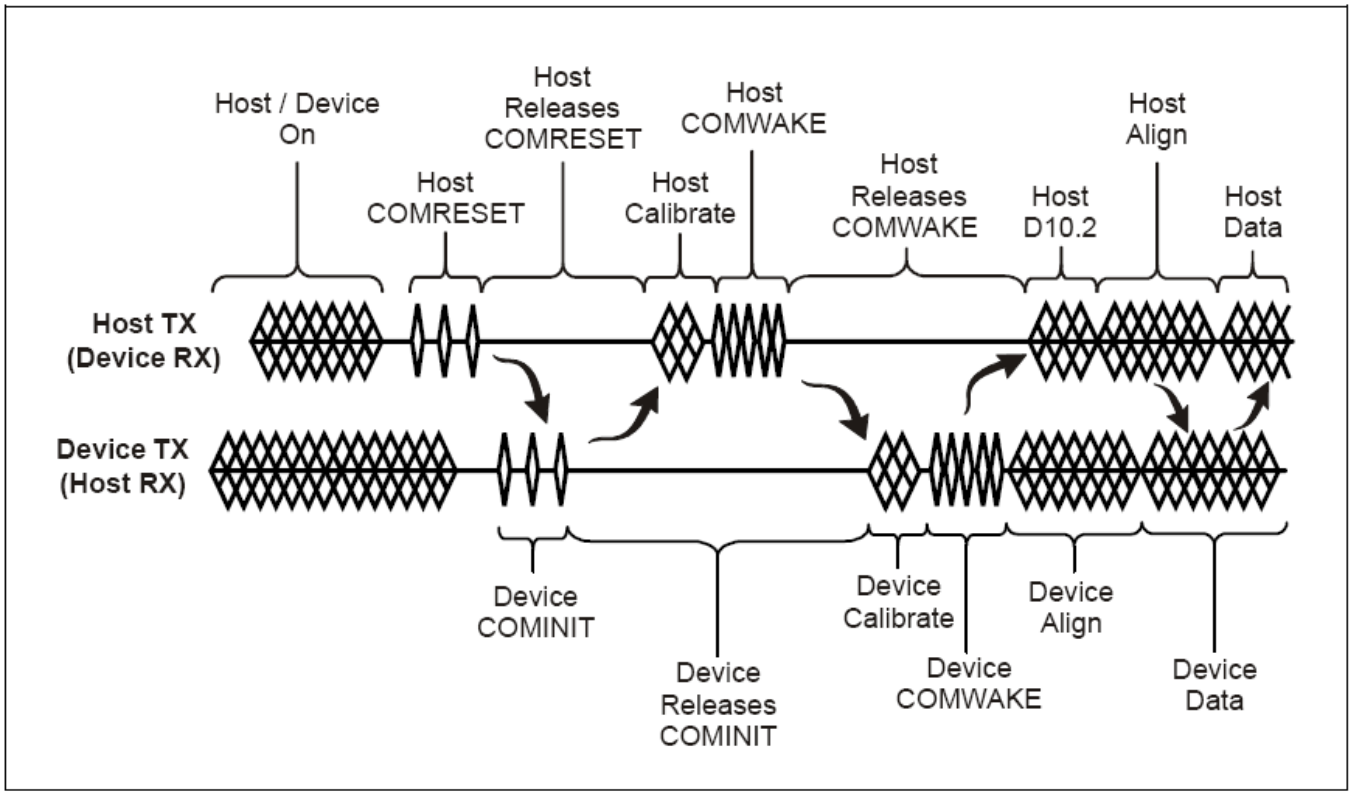


Figure 6 : comreset sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.

2. Some condition in the host causes the host to issue COMRESET

3. Host releases COMRESET. Once the condition causing the COMRESET is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.

4. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.

5. Host calibrates and issues a COMWAKE.

6. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error state.

7. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.

8. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.

9. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

9.3 COMINI

COMINIT always originates from the drive and requests a communication initialization. It is electrically identical to the COMRESET signal except that it originates from the device and is sent to the host. It is used by the device to request a reset from the host in accordance to the sequence shown in Figure 7, below.

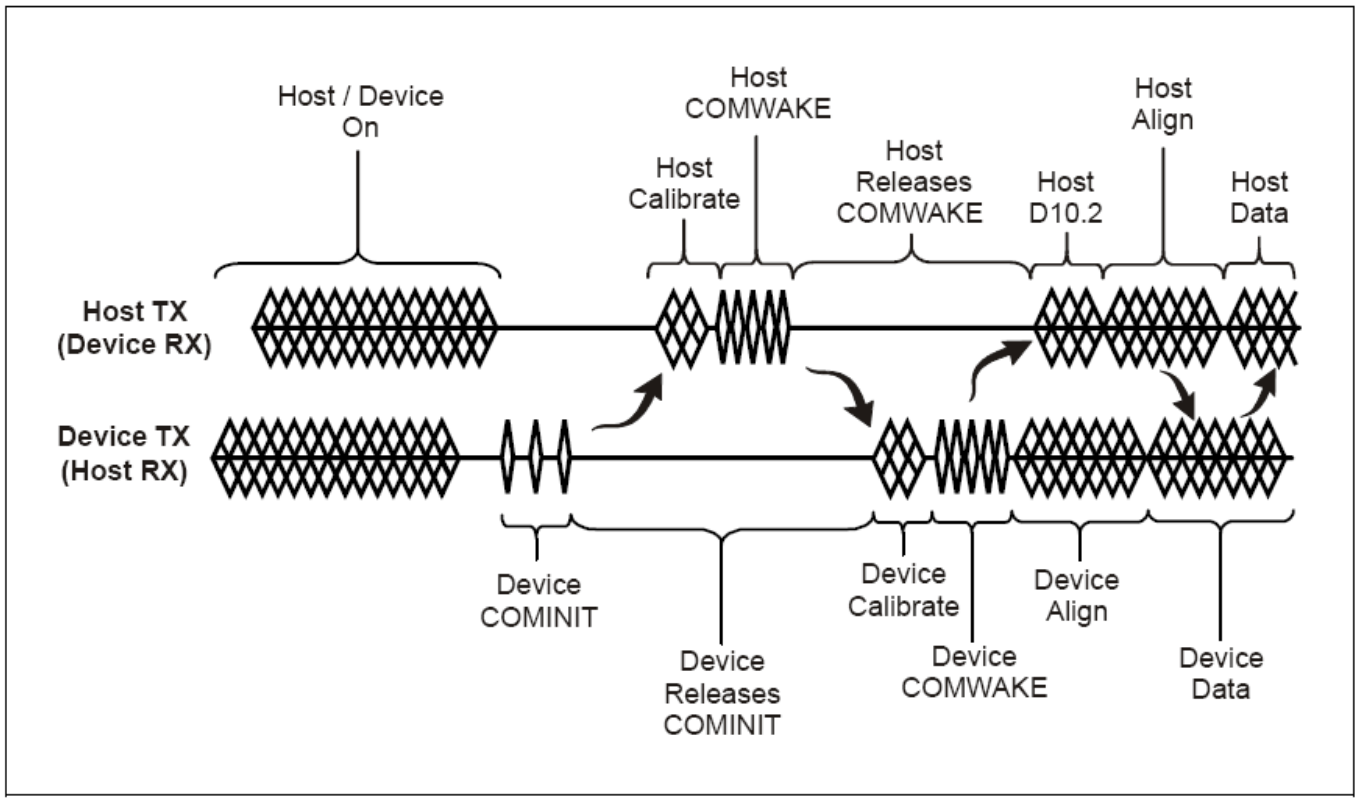


Figure 7 : cominit sequence

Description:

1. Host/device are powered and operating normally with some form of active communication.
2. Some condition in the device causes the device to issues a COMINIT
3. Host calibrates and issues a COMWAKE.
4. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP Dwords have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP Dwords at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device enters an error

state.

5. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see section 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This ensures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
6. Device locks – the device locks to the ALIGN sequence and, when ready, sends SYNCP indicating it is ready to start normal operation.
7. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

9.4 Power on sequence timing diagram

The following timing diagrams and descriptions are provided for clarity and are informative. The state diagrams provided in section 8.4 comprise the normative behavior specification and is the ultimate reference.

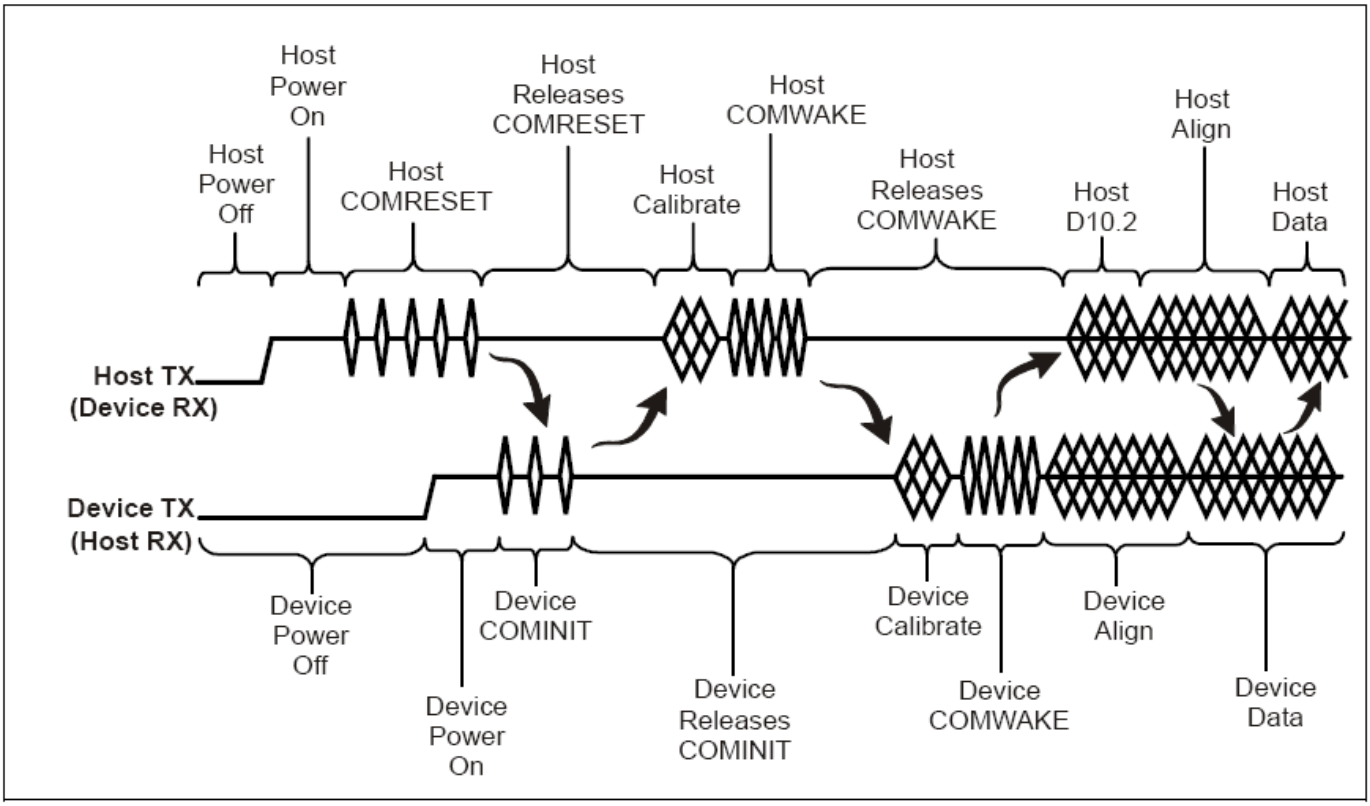


Figure 8 : power on sequence

Description:

1. Host/device power-off - Host and device power-off.
2. Power is applied - Host side signal conditioning pulls TX and RX pairs to neutral state (common mode voltage).
3. Host issues COMRESET
4. Host releases COMRESET. Once the power-on reset is released, the host releases the COMRESET signal and puts the bus in a quiescent condition.
5. Device issues COMINIT – When the device detects the release of COMRESET, it responds with a COMINIT. This is also the entry point if the device is late starting. The device may initiate communications at any time by issuing a COMINIT.
6. Host calibrates and issues a COMWAKE.
7. Device responds – The device detects the COMWAKE sequence on its RX pair and calibrates its transmitter (optional). Following calibration the device sends a six burst COMWAKE sequence and then sends a continuous stream of the ALIGN sequence starting at the device's highest supported speed. After ALIGNP primitives have been sent for 54.6 us (2048 nominal Gen1 Dword times) without a response from the host as determined by detection of ALIGNP primitives received from the host, the device assumes that the host cannot communicate at that speed. If additional speeds are available the device tries the next lower supported speed by sending ALIGNP primitives at that rate for 54.6 us (2048 nominal Gen1 Dword times.) This step is repeated for as many slower speeds as are supported. Once the lowest speed has been reached without response from the host, the device shall enter an error state.
8. Host locks – after detecting the COMWAKE, the host starts transmitting D10.2 characters (see 7.6) at its lowest supported rate. Meanwhile, the host receiver locks to the ALIGN sequence and, when ready, returns the ALIGN sequence to the device at the same speed as received. A host shall be designed such that it acquires lock in 54.6 us (2048 nominal Gen1 Dword times) at any given speed. The host should allow for at least 873.8 us (32768 nominal Gen1 Dword times) after detecting the release of COMWAKE to receive the first ALIGNP. This insures interoperability with multi-generational and synchronous designs. If no ALIGNP is received within 873.8 us (32768 nominal Gen1 Dword times) the host restarts the power-on sequence – repeating indefinitely until told to stop by the Application layer.
9. Device locks – the device locks to the ALIGN sequence and, when ready, sends the SYNCP primitive indicating it is ready to start normal operation.
10. Upon receipt of three back-to-back non-ALIGNP primitives, the communication link is established and normal operation may begin.

9.5 ATA command register

This table with the following paragraphs summarizes the ATA command set.

Command Table

Command Name	Code	PARAMETERS USED					
		SC	SN	CY	DR	HD	FT
CHECK POWER MODE	E5h	X	X	X	O	X	X
EXECUTE DIAGNOSTICS	90h	X	X	X	O	X	X
FLUSH CACHE	E7h	X	X	X	O	O	X
FLUSH CACHE EXT	EAh	X	X	X	O	O	X
IDENTIFY DEVICE	ECh	X	X	X	O	X	X
IDLE	E3h	O	X	X	O	X	X
IDLE IMMEDIATE	E1h	X	X	X	O	X	X
INITIALIZE DEVICE PARAMETERS	91h	O	X	X	O	O	X
READ BUFFER	E4H	X	X	X	O	X	X
READ DMA	C8h or C9h	O	O	O	O	O	X
READ DMA EXT	25h	O	O	O	O	O	X
READ FPDMA QUEUED	60h	O	O	O	O	O	O
READ LOG EXT	2Fh	O	O	O	O	O	O
READ MULTIPLE	C4h	O	O	O	O	O	X
READ MULTIPLE EXT	29h	O	O	O	O	O	X
READ SECTOR(S)	20h or 21h	O	O	O	O	O	X
READ SECTOR(S) EXT	24h	O	O	O	O	O	X
READ VERIFY SECTOR(S)	40h or 41h	O	O	O	O	O	X
READ VERIFY SECTOR(S) EXT	42h	O	O	O	O	O	X
RECALIBRATE	10h	X	X	X	O	X	X
SECURITY DISABLE PASSWORD	F6h	X	X	X	O	X	X
SECURITY ERASE PREPARE	F3h	X	X	X	O	X	X
SECURITY ERASE UNIT	F4h	X	X	X	O	X	X
SECURITY FREEZE LOCK	F5h	X	X	X	O	X	X
SECURITY SET PASSWORD	F1h	X	X	X	O	X	X
SECURITY UNLOCK	F2h	X	X	X	O	X	X
SEEK	7xh	X	X	O	O	O	X
SET FEATURES	EFh	O	X	X	O	X	O
SET MULTIPLE MODE	C6h	O	X	X	O	X	X
SLEEP	E6h	X	X	X	O	X	X

SMART	B0h	X	X	O	O	X	O
STANDBY	E2h	X	X	X	O	X	X
STANDBY IMMEDIATE	E0h	X	X	X	O	X	X
WRITE BUFFER	E8h	X	X	X	O	X	X
WRITE DMA	CAh or CBh	O	O	O	O	O	X
WRITE DMA EXT	35h	O	O	O	O	O	X
WRITE DMA FUA EXT	3Dh	O	O	O	O	O	X
WRITE FPDMA QUEUED	61h	O	O	O	O	O	O
WRITE MULTIPLE	C5h	O	O	O	O	O	X
WRITE MULTIPLE EXT	39h	O	O	O	O	O	X
WRITE MULTIPLE FUA EXT	CEh	O	O	O	O	O	X
WRITE SECTOR(S)	30h or 31h	O	O	O	O	O	X
WRITE SECTOR(S) EXT	34h	O	O	O	O	O	X

Note:

O = Valid, X = Don't care

SC = Sector Count Register

SN = Sector Number Register

CY = Cylinder Low/High Register

DR = DEVICE SELECT Bit (DEVICE/HEAD Register Bit 4)

HD = HEAD SELECT Bit (DEVICE/HEAD Register Bit 3-0)

FT = Features Register

ATA COMMAND SPECIFICATIONS

CHECK POWER MODE (E5h)

The host can use this command to determine the current power management mode.

EXECUTE DIAGNOSITICS (90h)

This command performs the internal diagnostic tests implemented by the drive. See ERROR register for dianostic codes.

FLUSH CACHE (E7h)

This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

FLUSH CACHE EXT (EAh)

48-bit feature set mandatory command. This command is used by the host to request the device to flush the write cache. If there is data in the write cache, that data shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs.

IDENTIFY DEVICE (ECh)

This commands read out 512Bytes of drive parameter information. Parameter Information consists of the arrangement and value as shown in the following table. This command enables the host to receive the Identify Drive Information from the device.

Identify Device Information Default Value

Word	Value	F/V	Description
0	0040h		General configuration bit-significant information:
		F	15 0 = ATA device
		X	14-8 Retired
		X	7-6 Obsolete
		X	5-3 Retired
		V	2 Reserved
		X	1 Retired
			0 Reserved
1	3FFFh	F	Number of logical cylinders
2	C837h	V	Specific configuration
3	0010h	F	Number of logical heads
4-5	0000h	X	Retired
6	003Fh	F	Number of logical sector per logical track
7-8	0000h		Reserved for assignment by the CompactFlash_ Association
9	0000h	X	Retired
10-19	XXXXh	F	Serial number (20 ASCII characters)
20-21	0000h	X	Retired
22	0000h	X	Obsolete
23-26	XXXXh	F	Firmware revision (8 ASCII characters)
27-46	XXXXh	F	Model number (40 ASCII characters)
47	8001h	F	15-8 80h
		F	7-0 00h = Reserved
		F	01h = Maximum number of 1 sectors on READ/WRITE MULTIPLE commands
48	0000h	F	Reserved
49	2F00h		Capabilities
			15-14 Reserved for the IDENTIFY PACKET DEVICE command.
		F	13 1 = Standby timer values as specified in this standard are supported
			0 = Standby timer values shall be managed by the device
			12 Reserved for the IDENTIFY PACKET DEVICE command.
		F	11 1 = IORDY supported
			0 = IORDY may be supported
		F	10 1 = IORDY may be disabled
		F	9 1 = LBA supported
		F	8 1 = DMA supported.
		X	7-0 Retired
50	4000h		Capabilities
		F	15 Shall be cleared to zero.
		F	14 Shall be set to one.
			13-2 Reserved.
		X	1 Obsolete
		F	0 Shall be set to one to indicate a device specific Standby timer value minimum.

Identify Device Information Default Value (*cont.*)

Word	Value	F/V	Description
51	0000h	F	15-8 PIO data transfer cycle timing mode 7-0 Reserved
52	0000h	X	Obsolete
53	0007h	F F F X	15-3 Reserved 2 1 = the fields reported in word 88 are valid 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words 70:64 are valid 0 = the fields reported in words 70:64 are not valid 0 1 = the fields reported in words 58:54 are valid 0 = the fields reported in words 58:54 are not valid
54	XXXXh	X	Number of current cylinders
55	00XXh	X	Number of current heads
56	XXXXh	X	Number of current sector per track
57-58	XXXXh	X	Current capacity in sectors
59	0101h	 V V	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	XXXXh	F	Total number of user addressable sectors
62	0000h	X	Obsolete
63	0007h	F V V V F F F	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected 9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported 1 1 = Multiword DMA mode 1 and below are supported 0 1 = Multiword DMA mode 0 is supported
64	0003h	 F	15-8 Reserved 7-0 Advanced PIO modes supported
65	0078h	F	Minimum Multiword DMA transfer cycle time per word
66	0078h	F	Manufacturer's recommended Multiword DMA transfer cycle time
67	0078h	F	Minimum PIO transfer cycle time without flow control
68	0078h	F	Minimum PIO transfer cycle time with IORDY flow control
69-70	0000h		Reserved
71-74	0000h		Reserved for the IDENTIFY PACKET DEVICE command
75	0000h	 F	Queue depth 15-5 Reserved 4-0 Maximum queue depth – 1

Identify Device Information Default Value (*cont.*)

Word	Value	F/V	Description
76	0206h		Serial ATA Capabilities
			15-11 Reserved for Serial ATA
		F	10 1 = Supports Phy Event Counts
		F	9 1 = Supports receipt of host initiated power management requests
		F	8 1 = Supports the NCQ feature set
			7-3 Reserved for Serial ATA
		F	2 1 = Supports SATA Gen2 Signaling Speed (3.0Gb/s)
		F	1 1 = Supports SATA Gen1 Signaling Speed (1.5Gb/s)
		F	0 Shall be cleared to zero
77	0000h		Reserved for Serial ATA
78	0008h		Serial ATA feature supported
			15-7 Reserved for Serial ATA
		F	6 1 = Device supports Software Settings Preservation
			5 Reserved for Serial ATA
		F	4 1 = Device supports in-order data delivery
		F	3 1 = Device supports initiating power management
		F	2 1 = Device supports DMA Setup auto-activation
		F	1 1 = Device supports non-zero buffer offsets
		F	0 Shall be cleared to zero
79	0000h		Serial ATA feature enabled
			15-7 Reserved for Serial ATA
		V	6 1 = Software Settings Preservation enabled
			5 Reserved for Serial ATA
		V	4 1 = In-order data delivery enabled
		V	3 1 = Device initiated power management enabled
		V	2 1 = DMA Setup auto-activation enabled
		V	1 1 = Non-zero buffer offsets enabled
		F	0 Shall be cleared to zero
80	00F0h		Major version number 0000h or FFFFh = device does not report version
			15 Reserved
		F	14 Reserved for ATA/ATAPI-14
		F	13 Reserved for ATA/ATAPI-13
		F	12 Reserved for ATA/ATAPI-12
		F	11 Reserved for ATA/ATAPI-11
		F	10 Reserved for ATA/ATAPI-10
		F	9 Reserved for ATA/ATAPI-9
		F	8 Reserved for ATA/ATAPI-8
		F	7 1 = supports ATA/ATAPI-7
		F	6 1 = supports ATA/ATAPI-6
		F	5 1 = supports ATA/ATAPI-5
		F	4 1 = supports ATA/ATAPI-4
		F	3 Obsolete
		X	2 Obsolete
		X	1 Obsolete
			0 Reserved
81	0000h	F	Minor version number

Identify Device Information Default Value (*cont.*)

Word	Value	F/V	Description
82	302Bh		Command and feature sets supported
		X	15 Obsolete
		F	14 1 = NOP command supported
		F	13 1 = READ BUFFER command supported
		F	12 1 = WRITE BUFFER command supported
		X	11 Obsolete
		F	10 1 = Host Protected Area feature set supported
		F	9 1 = DEVICE RESET command supported
		F	8 1 = SERVICE interrupt supported
		F	7 1 = release interrupt supported
		F	6 1 = look-ahead supported
		F	5 1 = write cache supported
		F	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3 1 = mandatory Power Management feature set supported
		F	2 1 = Removable Media feature set supported
		F	1 1 = Security Mode feature set supported
		F	0 1 = SMART feature set supported
83	5000h		Command and feature sets supported
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = The FLUSH CACHE EXT command is supported
		F	12 Shall be set to one to indicate that the mandatory FLUSH CACHE command is supported
		F	11 1 = The DCO feature set is supported
		F	10 1 = The 48-bit Address feature set is suported
		F	9 1 = The AAM feature set is supported
		F	8 1 = SET MAX security extension supported
			7 Reserved
		F	6 1 = SET FEATURES subcommand required to spinup after power-up
		F	5 1 = Power-Up In Standby feature set supported
		F	4 1 = Removable Media Status Notification feature set supported
		F	3 1 = Advanced Power Management feature set supported
		F	2 1 = CFA feature set supported
		F	1 1 = READ/WRITE DMA QUEUED supported
		F	0 1 = DOWNLOAD MICROCODE command supported
84	4000h		Command and feature sets supported
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = The IDLE IMMEDIATE command with UNLOAD feature is supported
			12-11 Reserved for TLC
		X	10-9 Obsolete
		F	8 1 = The 64-bit World wide name is supported
		F	7 1 = The WRITE DMA QUEUED FUA EXT command is supported
		F	6 1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
		F	5 1 = The GPL feature set is supported
		F	4 1 = The Streaming feature set is supported
		F	3 1 = The Media Card Pass Through Command feature set is supported
		F	2 1 = Media serial number is supported
		F	1 1 = SMART self-test supported
		F	0 1 = SMART error logging supported

Identify Device Information Default Value (*cont.*)

Word	Value	F/V	Description
85	3029h		Command and feature sets supported or enable
		X	15 Obsolete
		F	14 1 = The NOP command is supported
		F	13 1 = The READ BUFFER command is supported
		F	12 1 = The WRITE BUFFER command is supported
		X	11 Obsolete
		V	10 1 = HPA feature set is supported
		F	9 Shall be cleared to zero to indicate that the DEVICE RESET command is not supported
		V	8 1 = The SERVICE interrupt is enabled
		V	7 1 = The release interrupt is enabled
		V	6 1 = Read look-ahead is enabled
		V	5 1 = The volatile write cache is enabled
		F	4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.
		F	3 Shall be set to one to indicate that the mandatory Power Management feature is supported
		X	2 Obsolete
		V	1 1 = The Security feature set is enabled
		V	0 1 = The SMART feature set is enabled
86	1000h		Command and feature sets supported or enable
		F	15 1 = Words 119-120 are valid
			14 Reserved
		F	13 1 = FLUSH CACHE EXT command supported
		F	12 1 = FLUSH CACHE command supported
		F	11 1 = The DCO feature set is supported
		F	10 1 = The 48-bit Address feature set is supported
		V	9 1 = The AAM feature set is enable
		V	8 1 = The SET MAX security extension is enabled by SET MAX SET PASSWORD
			7 Reserved for Address Offset Reserved Area Boot Method
		F	6 1 = SET FEATURES subcommand required to spin-up after power-up
		V	5 1 = The PUIS feature set is enabled
		X	4 Obsolete
		V	3 1 = The APM feature set is enabled
		F	2 1 = The CFA feature set is supported
		F	1 1 = The TCQ feature set is supported
		F	0 1 = The DOWNLOAD MICROCODE command is supported
87	4000h		Command and feature sets supported or enabled
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = The IDLE IMMEDIATE command with UNLOAD feature is supported
			12-11 Reserved for TLC
		X	10-9 Obsolete
		F	8 1 = The 64-bit World wide name is supported
		F	7 1 = The WRITE DMA QUEUED FUA EXT command is supported
		F	6 1 = The WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands are supported
		F	5 1 = The GPL feature set is supported
		X	4 Obsolete
		V	3 1 = The Media Card Pass Through Command feature set is supported
		V	2 1 = Media serial number is supported
		F	1 1 = SMART self-test supported
		F	0 1 = SMART error logging supported

Identify Device Information Default Value (*cont.*)

Word	Value	F/V	Description
88	203Fh		Ultra DMA modes
			15 Reserved
		V	14 1 = Ultra DMA mode 6 is selected
			0 = Ultra DMA mode 6 is not selected
		V	13 1 = Ultra DMA mode 5 is selected
			0 = Ultra DMA mode 5 is not selected
		V	12 1 = Ultra DMA mode 4 is selected
			0 = Ultra DMA mode 4 is not selected
		V	11 1 = Ultra DMA mode 3 is selected
			0 = Ultra DMA mode 3 is not selected
		V	10 1 = Ultra DMA mode 2 is selected
			0 = Ultra DMA mode 2 is not selected
		V	9 1 = Ultra DMA mode 1 is selected
			0 = Ultra DMA mode 1 is not selected
		V	8 1 = Ultra DMA mode 0 is selected
			0 = Ultra DMA mode 0 is not selected
			7 Reserved
		F	6 1 = Ultra DMA mode 6 and below are supported
		F	5 1 = Ultra DMA mode 5 and below are supported
		F	4 1 = Ultra DMA mode 4 and below are supported
		F	3 1 = Ultra DMA mode 3 and below are supported
		F	2 1 = Ultra DMA mode 2 and below are supported
		F	1 1 = Ultra DMA mode 1 and below are supported
		F	0 1 = Ultra DMA mode 0 is supported
89	0001h		15-8 Reserved
		F	7-0 Time required for Normal Erase mode SECURITY ERASE UNIT command
90	0001h		15-8 Reserved
		F	7-0 Time required for Enhanced Erase mode SECURITY ERASE UNIT command
91	0000h	V	Current APM level value
92	FFFEh	V	Master Password Identifier
93	0000h	X	Hardware reset result
94	0000h		Current AAM value
		F	15-8 Vendor's recommended AAM value
		V	7-0 Current AAM value
95-99	0000h		Reserved
100-103	XXXXh	X	Total Number of User Addressable Logical Sectors for 48-bit commands (QWord)
104-105	0000h		Reserved
106	4000h		Physical sector size / logical sector size
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
		F	13 1 = Device has multiple logical sectors per physical sector
		F	12 1 = Device Logical Sector longer than 256 Words
			11-4 Reserved
		F	3-0 2x logical sectors per physical sector
107-118	0000h		Reserved

Identify Device Information Default Value (*cont.*)

Word	Value	F/V	Description
119	4000h		Commands and feature sets supported (Continued from words 84:82)
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
			13-6 Reserved
		F	5 1= The Free-fall Control feature set is supported
		F	4 1 = The DOWNLOAD MICROCODE command with mode 3 is supported
		F	3 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported
		F	2 1 = The WRITE UNCORRECTABLE EXT command is supported
		F	1 1 = The Write-Read-Verify feature set is supported
			0 Reserved for DDT
120	4000h		Commands and feature sets supported or enabled (Continued from words 87:85)
		F	15 Shall be cleared to zero
		F	14 Shall be set to one
			13-6 Reserved
		V	5 1= The Free-fall Control feature set is enabled
		F	4 1 = The DOWNLOAD MICROCODE command with mode 3 is supported
		F	3 1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported
		F	2 1 = The WRITE UNCORRECTABLE EXT command is supported
		V	1 1 = The Write-Read-Verify feature set is enabled
			0 Reserved for DDT
121-126	0000h		Reserved for expended supported and enabled settings
127	0000h	X	Obsolete
128	0021h		Security status
		F	15-9 Reserved
		V	8 Security level 0 = High, 1 = Maximum
		F	7-6 Reserved
		F	5 1 = Enhanced security erase supported
		V	4 1 = Security count expired
		V	3 1 = Security frozen
		V	2 1 = Security locked
		V	1 1 = Security enabled
		F	0 1 = Security supported
129-159	0000h	X	Vendor specific
160-216	0000h		Reserved
217	0001h	F	Nominal media rotation rate
218-254	0000h		Reserved
255	0000h	X	Integrity word
			15-8 Checksum
			7-0 Signature

Key:
F/V = Fixed/variable content
F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = the content of the word may be fixed or variable.

IDLE (E3h)

This command causes the device to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If sector count is non-zero, the automatic power down mode is enabled. If the sector count is zero, the automatic power mode is disabled.

IDLE IMMEDIATE (E1h)

This command causes the device to set BSY, enter the Idle(Read) mode, clear BSY and generate an interrupt.

INITIALIZE DEVICE PARAMETERS (91h)

This command enables the host to set the number of sectors per track and the number of tracks per heads.

READ BUFFER (E4h)

The READ BUFFER command enables the host to read a 512-byte block of data.

READ DMA (C8h)

Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 256 sectors.

READ DMA EXT (25h)

48-bit feature set mandatory command. Read data from sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value. A sector count of zero requests 65536 sectors.

READ FPDMA QUEUED (60h)

NCQ feature set mandatory 48-bit command. This command requests that data to be transferred from the device to the host.

READ LOG EXT (2Fh)

General purpose logging feature set mandatory 48-bit command. This command returns the specified log to the host.

Log Address	Log Name	Feature Set	R/W	Access
00h	Log directory	N/A	RO	GPL
10h	NCQ Command Error	NCQ	RO	GPL

READ MULTIPLE (C4h)

This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ MULTIPLE EXT (29h)

48-bit feature set mandatory command. This command performs similarly to the Read Sectors command. Interrupts are not generated on each sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

READ SECTOR(S) (20h/21h)

This command reads 1 to 256 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of 0 requests 256 sectors. The transfer beings specified in the Sector Number register.

READ SECTOR(S) EXT (24h)

48-bit feature set mandatory command. This command reads 1 to 65536 sectors as specified in the Sector Count register from sectors which is set by Sector number register. A sector count of zero requests 65536 sectors. The transfer beings specified in the Sector Number register.

READ VERIFY SECTOR(S) (40h/41h)

This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

READ VERIFY SECTOR(S) EXT (42h)

48-bit feature set mandatory command. This command verifies one or more sectors on the drive by transferring data from the flash media to the data buffer in the drive and verifying that the ECC is correct. This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host.

RECALIBRATE (10h)

The current drive performs no processing if it receives this command. It is supported for backward compatibility with previous devices.

SECURITY DISABLE PASSWORD (F6h)

Disables any previously set user password and cancels the lock. The host transfers 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY ERASE PREPARE (F3h)

This command shall be issued immediately before the Security Erase Unit command to enable erasing and unlocking. This command prevents accidental loss of data on the drive.

SECURITY ERASE UNIT (F4h)

The host uses this command to transfer 512 bytes of data, as shown in the following table, to the drive. The transferred data contains a user or master password, which the drive compares with the saved password. If they match, the drive deletes user data, disables the user password, and cancels the lock. The master password is still saved. It is re-enabled by issuing the SECURITY SET PASSWORD command to re-set a user password.

SECURITY FREEZE LOCK (F5h)

Causes the drive to enter Frozen mode. Once this command has been executed, the following commands to update a lock result in the Aborted Command error:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

The drive exits from Frozen mode upon a power-off or hard reset. If the SECURITY FREEZE LOCK command is issued when the drive is placed in Frozen mode, the drive executes the command, staying in Frozen mode.

SECURITY SET PASSWORD (F1h)

This command set user password or master password. The host outputs sector data with PIO data-out protocol to indicate the information defined in the following table.

SECURITY UNLOCK (F2h)

This command disable LOCKED MODE of the device. This command transfers 512 bytes of data from the host with PIO data-out protocol. The following table defines the content of this information.

SEEK (7xh)

This command is effectively a NOP command to the device although it does perform a range check.

SET FEATURES (EFh)

This command set parameter to Features register and set drive's operation. For transfer mode, parameter is set to Sector Count register. This command is used by the host to establish or select certain features.

Features register Value and settable operating mode

Value	Function
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register.
55h	Disable read look-ahead feature
82h	Disable write cache
AAh	Enable read look-ahead feature

SET MULTIPLE MODE (C6h)

This command enables the device to perform READ MULTIPLE and WRITE MULTIPLE operations and establishes the block count for these commands.

SLEEP (E6h)

This command causes the device to set BSY, enter the Sleep mode, clear BSY and generate an interrupt.

SMART Function Set (B0h)

Performs different processing required for predicting device failures, according to the subcommand specified in the Features register. If the Features register contains an unsupported value, the Aborted Command error is returned. If the SMART function is disabled, any subcommand other than SMART ENABLE OPERATIONS results in the Aborted Command error.

Code	Smart Subcommand
D0h	READ DATA
D1h	READ ATTRIBUTE THRESHOLDS
D2h	ENABLE/DISABLE ATTRIBUTE AUTOSAVE
D3h	SAVE ATTRIBUTE VALUES
D4h	EXECUTE OFF-LINE IMMIDIATE*
D5h	Reserved
D6h	Reserved
D8h	ENABLE OPERATIONS
D9h	DISABLE OPERATIONS
DAh	RETURN STATUS
DBh	ENABLE/DISABLE AUTO OFF-LINE*

*JMF60X not support.

SMART READ DATA

This command returns 512-byte SMART Data Structure to the host with PIO data-in protocol. The register file has to contain D0h for Features register, 4Fh for LBA Mid register and C2h for the LBA High register.

Byte	Description
0-1	Data structure revision number
2-13	1st attribute data
14-361	2nd-30th Individual attribute data
362	Off-line data collection status
363	Reserved
364-365	Total time in seconds to complete off-line data collection
366	Reserved
367	Off-line data collection capability
368-369	SMART capability
370-385	Reserved
386-510	Reserved
511	Data structure Checksum

Byte 2-361: Individual attribute data

Byte	Description
0	Attribute ID
1-2	Status Flag (0x0002)
3	Attribute Value (0x64)
4-11	Vendor Specific

The attribute ID information is listed in the following table

ID	Description	Detail Information	
		Byte	Description
E5h	Halt System ID, Flash ID	0	Halt System ID
		1	Flash ID (byte 1)
		2	Flash ID (byte 2)
		3	Flash ID (byte 3)
		4	Flash ID (byte 4)
		5	Flash ID (byte 5)

		6	Flash ID (byte 6)
		7	Flash ID (byte 7)
E8h	Firmware version information	0	Year (High Byte, ASCII)
		1	Year (Low Byte, ASCII)
		2	Month (High Byte, ASCII)
		3	Month (Low Byte, ASCII)
		4	Day (High Byte, ASCII)
		5	Day (Low Byte, ASCII)
		6	Channels (binary)
		7	Banks (binary)
E9h	ECC Fail Record	0	ECC fail number
		1	Row address 3
		2	Row address 2
		3	Row address 1
		4	Channel number of last ECC fail
		5	Bank number of last ECC fail
		6	Reserved
		7	Reserved
EAh	Average Erase Count, Max Erase Count	0	Average Erase Count (High Byte)
		1	Average Erase Count
		2	Average Erase Count (Low Byte)
		3	Max Erase Count (High Byte)
		4	Max Erase Count
		5	Max Erase Count (Low Byte)
		6	Reserved
		7	Reserved
EBh	Good Block Count, System Block Count	0	Good Block Count (High Byte)
		1	Good Block Count
		2	Good Block Count (Low Byte)
		3	System(Free) Block Count (High Byte)
		4	System(Free) Block Count (Low Byte)
		5	Reserved
		6	Reserved
		7	Reserved
ECh-FFh	Reserved		

SMART READ ATTRIBUTE THRESHOLD

This transfers 512 bytes of drive failure threshold data to the host.

SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

Enables or disables the attribute value autosave function. This command specifies whether the current attribute values are automatically saved to the drive when it changes the mode. This setting is maintained when the power is turned on and off.

SMART SAVE ATTRIBUTE VALUE

Saves any modified attribute values.

SMART EXECUTE OFF-LINE IMMEDIATE

This command of Non-data input causes the controller to immediately initiate the set of activities that collect SMART data in a off-line mode and then save data to the Nand flash memory, or execute a selfdiagnostic test routine in either captive or off-line mode.

SMART ENABL OPERATIONS

Enables the SMART function. This setting is maintained when the power is turned off and then back on. Once the SMART function is enabled, subsequent SMART ENABLE OPERATIONS commands do not affect any parameters.

SMART DISABLE OPERATIONS

Disables the SMART function. Upon receiving the command, the drive disables all SMART operations. This setting is maintained when the power is turned off and then back on.

Once this command has been received, all SMART commands other than SMART ENABLE OPERATIONS are aborted with the Aborted Command error.

This command disables all SMART capabilities including any and all timer and event count functions related exclusively to this feature. After command acceptance, this controller will disable all SMART operations. SMART data in no longer be monitored or saved. The state of SMART is preserved across power cycles.

SMART RETURN STATUS

Reports the drive reliability status.

Values reported when a predicted defect has not been detected:

Cylinder Low register: 4Fh

Cylinder High register: C2h

Values reported when a predicted defect has been detected:

Cylinder Low register: F4h

Cylinder High register: 2Ch

SMART ENABLE/DISABLE AUTOMATIC OFF-LINE

Enables (when Sector Count register = “F8h”) or disables (Sector Count register = “00h”) the automatic off-line data collection function.

The automatic collection is disabled if a value of “00h” is set in the Sector Count register before a subcommand is issued. If automatic collection is disabled, the drive can still save attribute information during normal operation, such as during the power-on/off sequence or error correction sequence.

The automatic collection function is enabled if a value of “F8h” is set in the Sector Count register before the command is issued. Values other than “00h” and “F8h” are vendor-specific.

STANDBY (E2h)

This command causes the device to set BSY, enter the Sleep mode (which corresponds to the ATA“Standby” Mode), clear BSY and return the interrupt immediately.

STANDBY IMMEDIATE (E0h)

This command causes the drive to set BSY, enter the Sleep mode (which corresponds to the ATA “Standby” Mode), clear BSY and return the interrupt immediately.

WRITE BUFFER (E8h)

This command enables the host to write the contents of one 512-byte block of data to the device’s buffer.

WRITE DMA (CAh)

Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE DMA EXT (35h)

48-bit feature set mandatory command. Write data to sectors during Ultra DMA and Multiword DMA transfer. Use the SET FEATURES command to specify the mode value.

WRITE DMA FUA EXT (3Dh)

48-bit feature set mandatory command. This command provides the same function as the WRITE DMA EXT command except that regardless of whether volatile and/or non-volatile write caching in the device is enabled or not, the user data shall be written to non-volatile media before command completion is reported.

WRITE FPDMA QUEUED (61h)

NCQ feature set mandatory 48-bit command. This command causes data to be transferred from the host to the device.

WRITE MULTIPLE (C5h)

This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE MULTIPLE EXT (39h)

48-bit feature set mandatory command. This command is similar to the Write Sectors command. Interrupts are not presented on each sector, but on the transfer of a block which contains the number of sectors defined by Set Multiple command.

WRITE MULTIPLE FUA EXT (CEh)

48-bit feature set mandatory command. This command provides the same functionality as the WRITE MULTIPLE EXT command except that regardless of whether volatile and/or non-volatile write caching in the device is enabled or not, the user data shall be written to non-volatile media before command completion is reported.

WRITE SECTOR(S) (30h/31h)

Write data to a specified number of sectors (1 to 256, as specified with the Sector Count register) from the specified address. Specify “00h” to write 256 sectors.

WRITE SECTOR(S) EXT (34h)

48-bit feature set mandatory command. Write data to a specified number of sectors (1 to 65536, as specified with the Sector Count register) from the specified address. Specify “00h” to write 65536 sectors.

10. Electrical Characteristics

10.1 Absolute Maximum Rating

Parameter	Symbol	Condition	Min	Max	Unit
Analog power supply	AVDDH		-0.5	6	V
Digital I/O power supply	DVDD		-0.5	6	V
Digital I/O input voltage	$V_{I(D)}$		-0.4	DVDD+0.4	V
Storage temperature	$T_{STORAGE}$		-55	140	°C

10.2 Recommended Power Supply Operation Conditions and Temperature

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Operation digital power supply	PV33		3.0	3.3	3.6	V
	D1V8		1.85	1.9	2.0	V
Operation analog power supply	ASV33		3.0	3.3	3.6	V
	ASV18		1.85	1.9	2.0	V
	AVDDH		3.0	3.3	3.6	V
Ambient operation temperature	T_A	For commercial spec.	0		70	°C
Ambient operation temperature	T_A	For industry spec.	-40		85	°C
Junction temperature	T_J				125	°C
Case operation temperature	T_c	For commercial spec and base on T_A			85	°C
Case operation temperature	T_c	For industry spec and base on T_A			100	°C
TFBGA 211 ball 12X12	θJC			6.30		°C/W
TFBGA 211 ball 12X12	θJA			28.50		°C/W

10.3 Recommended External Clock Source Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Unit
External reference clock				30		MHz
Clock Duty Cycle			45	50	55	%

10.4 Power Supply DC Characteristics (SATA Idle mode)

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Digital power supply	I_{PV33}	3.3V		6		mA
	I_{DV18}	1.9V		94		mA
USB Analog Power Supply	I_{AVDDH}	3.3V		34		mA

Parameter	Symbol	Condition	Min	Typical	Max	Unit
SATA Analog Power Supply	I_{ASV33}	3.3V		2		mA
	I_{ASV18}	1.9V		120		mA

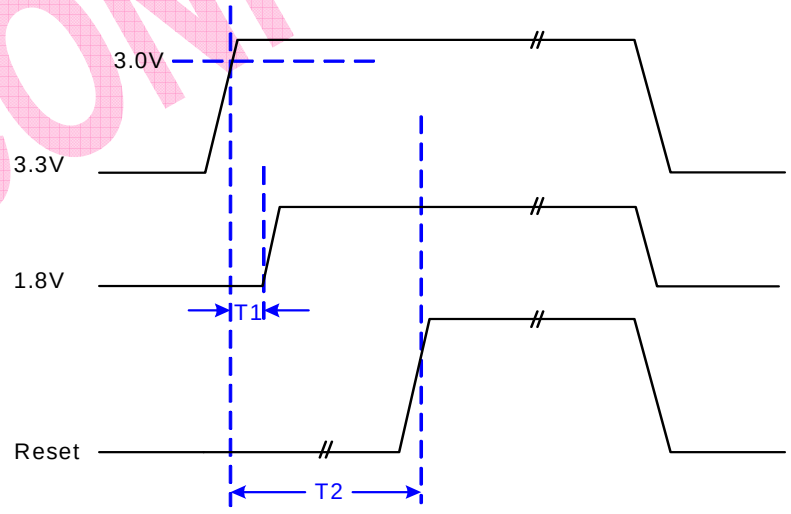
10.5 I/O DC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
Input low voltage	V_{IL}				0.8	V
Input high voltage	V_{IH}		2.0			V
Output low voltage	V_{OL}		0		0.4	V
Output high voltage	V_{OH}		2.6		3.6	V

10.6 Power Sequence

If external power design is applied, designers should make sure that the 3.3V power rail ramps prior to the 1.8V power rail or at the same time to prevent excessive current leakage. Except for 1.8V power rail, reset signal should be also taken into consideration. Designers should make sure that the 3.3V power rail ramps prior to the reset signal for system normal operating purpose. It is not acceptable if reset signal ramps prior to 3.3V power rail.

If internal power design is applied, 3.3V power rail will ramp prior to or simultaneously with the 1.8V power rail to prevent excessive current leakage onto the 3.3V power rail.



T1>= 0ms
T2> 10ms